IJREAT International Journal of Research in Engineering & Advanced Technology, Volume 1, Issue 4, Aug-Sept, 2013
ISSN: 2320 - 8791
www.ijreat.org

Digital design of Low power CMOS D-Latch basic

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Abstract: The main concern in VLSI Design is low power design, it is one of the various building blocks in digital design. The most basic block is the flip-flop in any digital memory circuit and it is used as memory element. In this paper, different types of CMOS technologies are designed and compared in terms of the impact of power on the D-latch basic. Power details are obtained from analog simulation to measure the power variations caused by various CMOS technologies.

Keywords: ***D-Latch-basic, CMOS, Power.***

I. INTRODUCTION:

The basic principle of the MOS field-effect transistor was explained by J. Lilienfeld in 1925, commercial success of MOS devices could be ensured only during the 1960s with the invention of the silicon planar process. Over the past two decades, Complementary Metal Oxide Silicon (CMOS) technology has played a very important role in the global integrated circuit industry. Nevertheless, the nMOS devices, fabricated by the nMOS-silicon-gate technology, came to be used in the early 1970s, prior to which only single-polarity p-type transistors were in use. At the same time, P.K. Weimer and F. Wanlass demonstrated the possibility of using both polarity devices on the same substrate. With the implementation of the CMOS inverter, NOR gate and NAND gate, initially using discrete transistors however, the CMOS concept took root, demonstrating the low power dissipation characteristics. Initially, requirement of more complex processing technology and larger silicon area compared to the single polarity transistors led to limited application of CMOS transistors to general system designs. However, as CMOS technology rapidly improved to support large chip sizes, and the issue of power consumption became more and more critical, CMOS technology has firmly established itself as the dominant VLSI technology. The total power dissipation is given by

$$P_{total} = P_{switching} + P_{SC} + P_{leakage}$$

Where P_{total} is the total power dissipation of a CMOS circuit, $P_{switching}$ is the switching power, P_{SC} is the short circuit power, and $P_{leakage}$ is the leakage power.

II. Overview of D Latch:

D latches are often used in I/O ports of integrated circuits and are available as discrete devices, often multiply packaged. An example is the 74HC75, part of the 7400 series of ICs, containing four separate D latches. Figure 1, represents the circuit diagram of D-latch basic or Transparent latch . It has two inputs D and E. and two outputs Q & Qbar. Latch is an electronic device that can be used to store one bit of information. The D latch is used to capture, or 'latch' the logic level which is present on the Data line when the clock input is high. If the data on the D line changes state while the clock pulse is high, then the output, Q, follows the input, D. When the CLK input falls to logic 0, the last state of the D input is trapped and held in the latch.

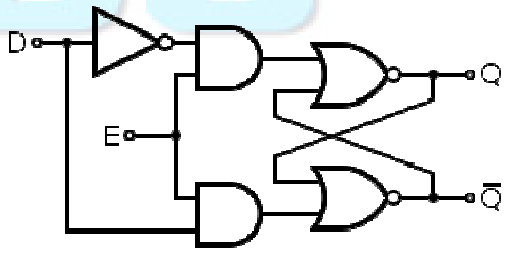


Figure 1.

III. Circuit operation:

The D latch outputs the *D* input whenever the *Enable* line is high, otherwise the output is whatever the *D* input was when the *Enable* input was last high. This is why it is also known as a transparent latch - when *Enable* is asserted, the latch is said to be "transparent" - it signals propagate directly through it as if it isn't there.

The timing diagram is as shown in figuree2.

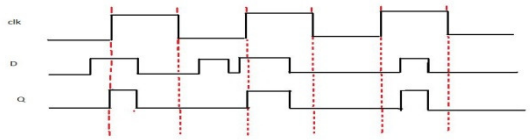


Figure 2.

A latch is an example of a bistable-multivibrator, that is, a device with exactly two stable states. These states are high-output and low-output. A latch has a feedback path, so information can be retained by the device. Therefore latches can be memory devices, and can store one bit of data for as long as the device is powered. As the name suggests, latches are used to "latch onto" information and hold in place. Latches are very similar to flip-flops, but are not synchronous devices, and do not operate on clock edges as flip-flops do.

Function table of D-latch.

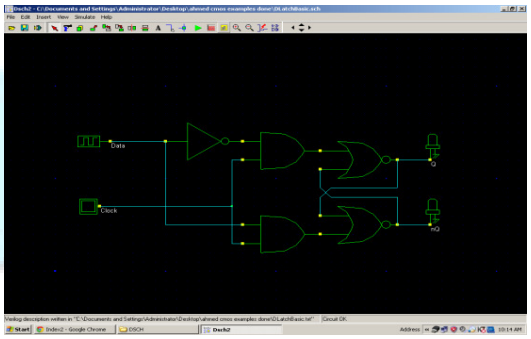
Table 1

Clock	Data	Q	nQ
0	0	LATCH	
0	1		
1	0	0	1
1	1	1	0

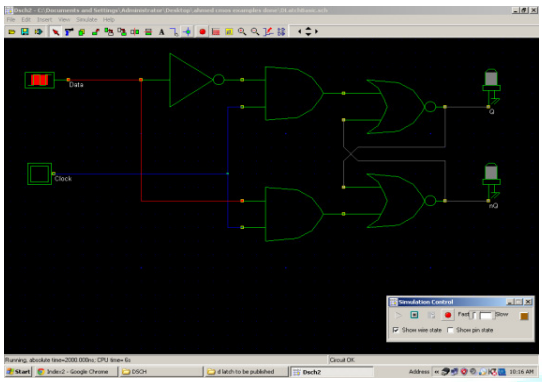
In this paper we present the implementation of CMOS D-latch basic with technologies like 0.12 µm , 0.8 µm, 0.6 µm with anlog simulation and power details.

IV. IMPLEMENTATION:

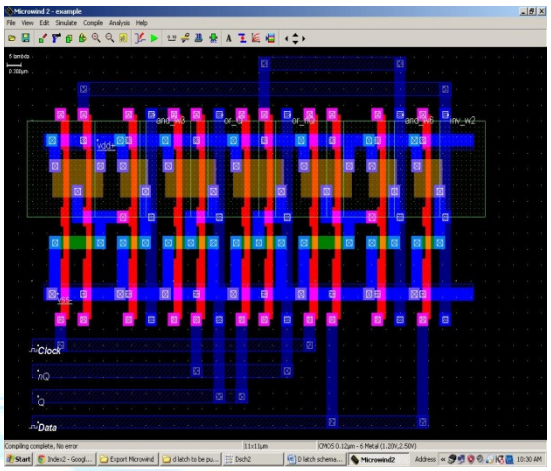
D-latch basic with out any inputs



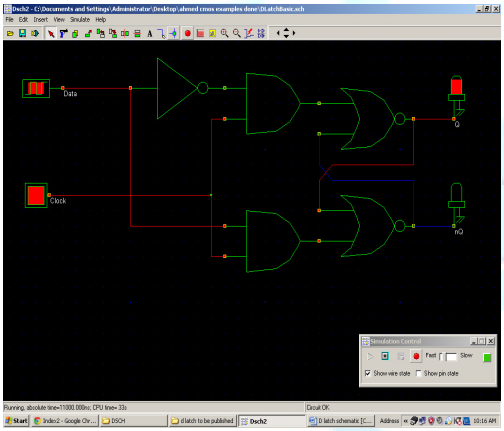
D-latch basic with D as input



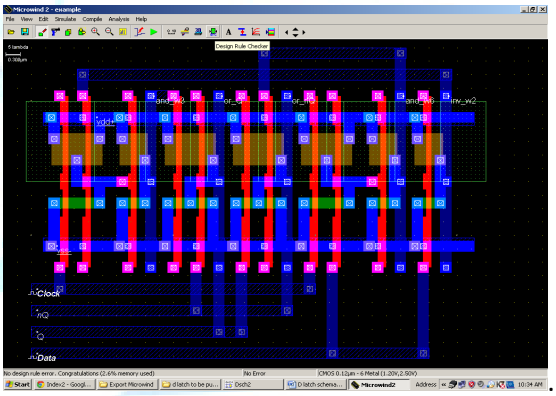
D-latch basic with D and Clock as inputs



The Design Rule check is passed with memory usage of 2.6%

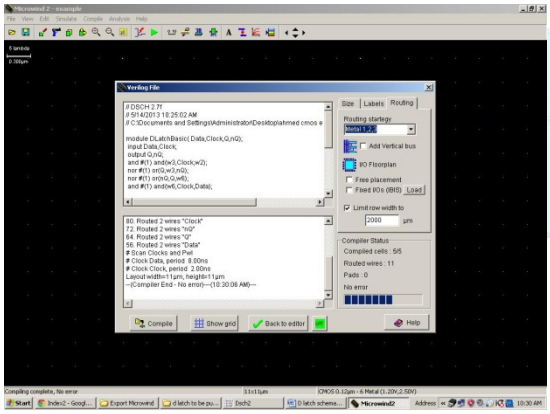


The verilog file created is

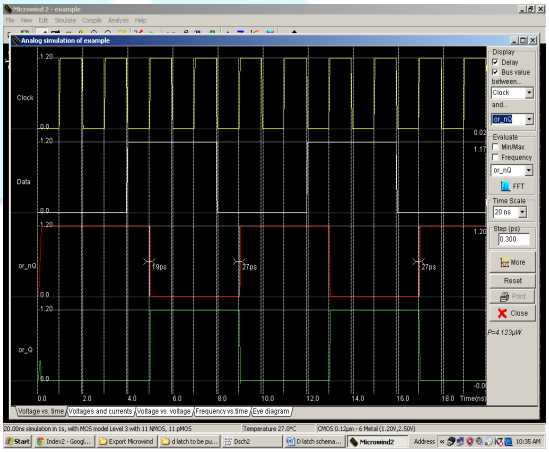


Analog simulation

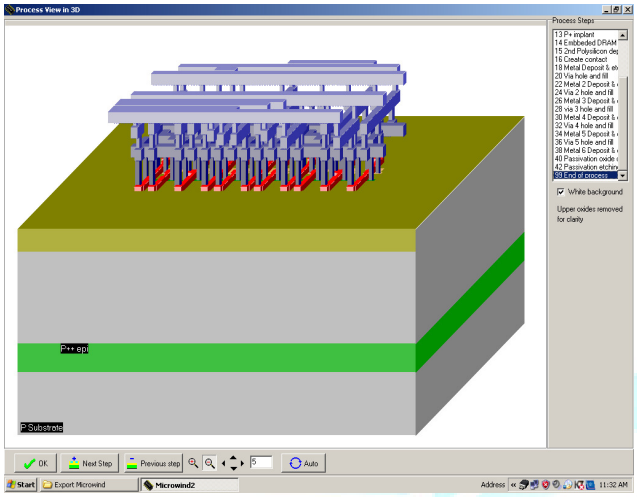
Power Dissipation using 0.12µm technology is 4.123µw



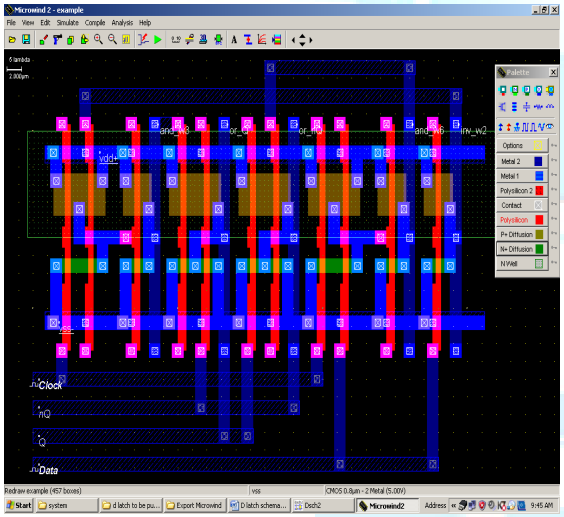
Layout of D-latch basic using 0.12µm technology



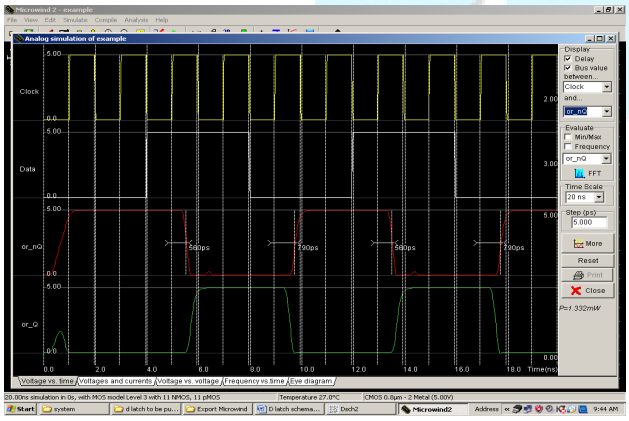
3D view of circuit is



Layout of D-latch basic using 0.8µm technology

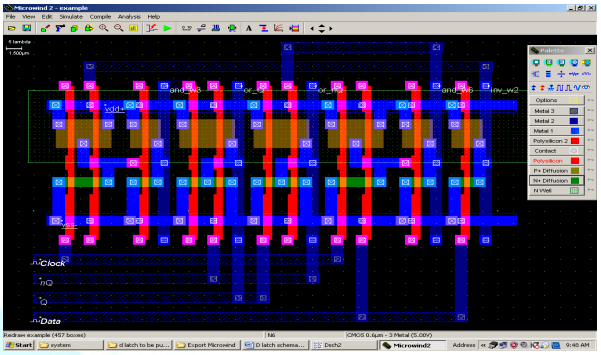


Analog simulation

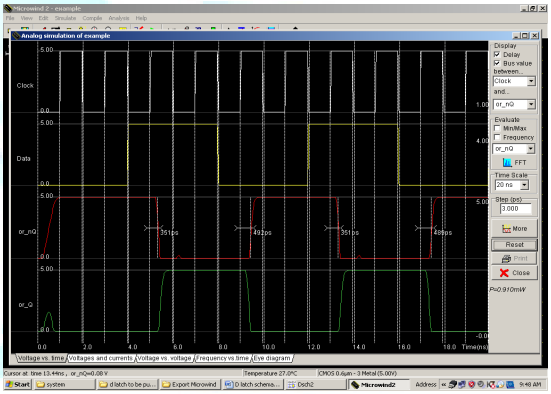


Power Dissipation using 0.8µm technology is 1.332mw

Layout of D-Latch basic using 0.6 µm technology



Analog simulation



Power Dissipation using 0.6µm technology is 0.910mw

V. Results:

In this paper power details are noted for technologies like 012um,0.8um,0.6um. the power details are reduced drastically in the case of 0.6um technology. A tabular column is created with comparisons of these three technologies with implementation D-Latch basic.

Technology	Lambda (λ)	No. of metals	V_{dd}	Power
0.12µm	0.6	6	1.2 to 2.5	4.123µw
0.8µm	0.4	2	5	1.332mw
0.6µm	0.3	3	5	0.91mw

VI. Conclusion and Future Scope:

In this paper we designed D-Latch basic and compared power of various technologies along with lambda, number of metals. Power dissipation can be still reduced by using advanced technologies.

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